Microcontrolador

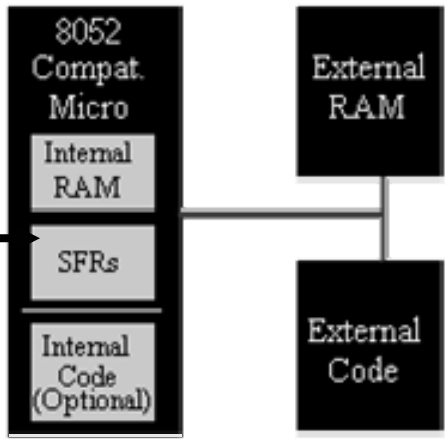
- MCU
  - Microcomputadora en un solo circuito que cumple funciones de CONTROL

Filosofía del bit

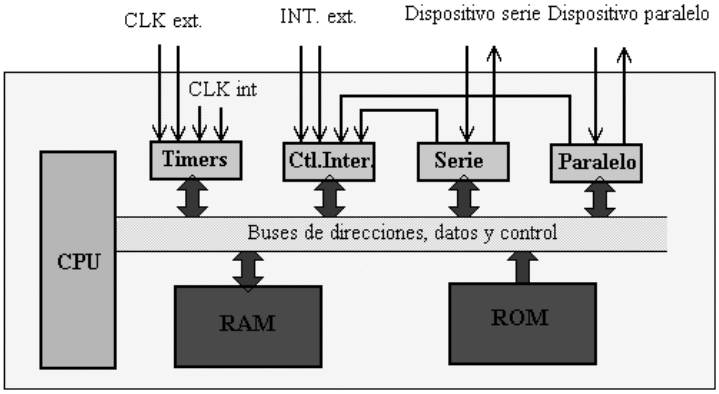
```
MOV   C,P1.4    ;Se trae al CY el estado del pin 4 de la puerta 1
ANL   C,P1.5    ;AND lógico con el estado de la pata 5 del port 1
ANL   C,P1.6    ;AND lógico del reultado anterior con el estado
                ;de la pata 6 del port 1
CPL   C         ;Se complementa el resultado
MOV   P1.7,C    ;Se escribe el resultado a la pata 7 del port 1
```

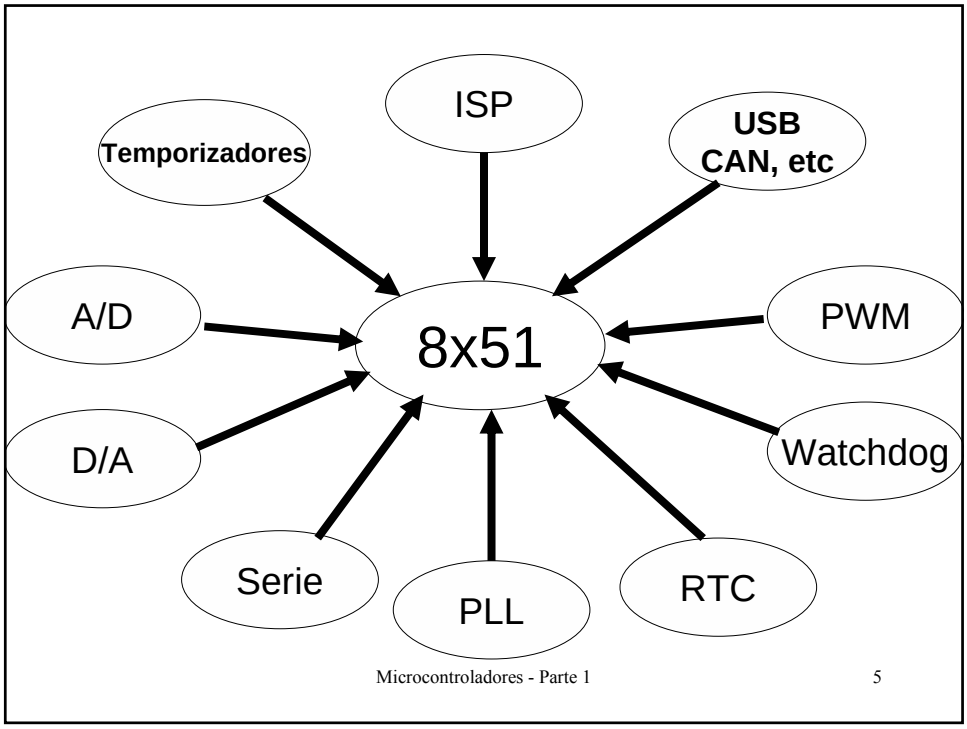
Microcontrolador

Registros de Funciones Especiales



Arquitectura



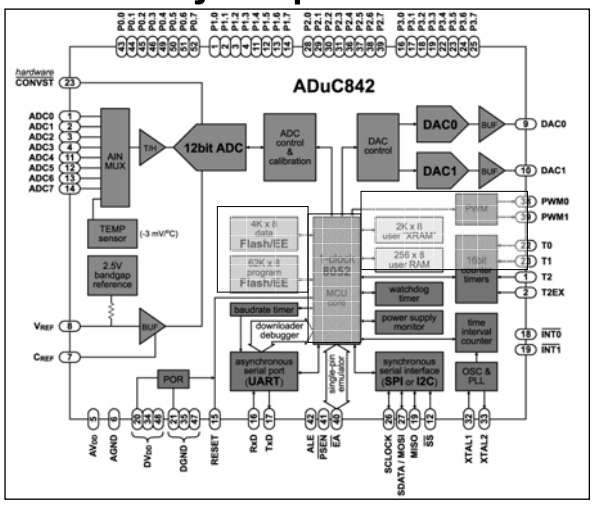


Ejemplos de Familias

High End	AT89C51...					
	RB2	RC2 / IC2	RD2 / ED2 / ID2	15	AC2	AC3
Pins	40/44	40/44	44/64	24/32	44	44
Flash (KB)	16	32	64	16	32	32
Mask ROM	Yes	Yes	Yes	-	-	-
SRAM (B)	1280	1280	2048	512	1280	2304
EEPROM (KB)	-	-	2 (ED2 / ID2)	2	2	2
U(S)ART	1	1	1	1	1	1
SPI	Yes	Yes	Yes	-	-	Yes
TWI	-	IC2	ID2	-	-	-
ADC	-	-	-	10 b	10b	10b
Keyboard	Yes	Yes	Yes	-	-	-
Timers	3	3	3	3	3	3
PCA / PWM	Yes	Yes	Yes	Yes	Yes	Yes
Watchdog	Yes	Yes	Yes	Yes	Yes	Yes
POR / PFD	-	-	Yes	-	-	Yes
ISP	Yes	Yes	Yes	Yes	Yes	Yes
Self Program.	Yes	Yes	Yes	Yes	Yes	Yes
Samples	Now	Now	Now	Now	Now	Now
Production	Now	Now	Now	Now	Now	Now

Part #	ADC	DAC	MCU	Flash/EE Code	Flash/EE Data	RAM	PKGs	Special Features
ADuC812	8-chan 12-bit	Dual 12-bit	12-clock 8052	8K-byte	640-byte	256-byte	52-PQFP 56-CSP	5µs ADC
ADuC814	6-chan 12-bit	Dual 12-bit	12-clock 8052	8K-byte	640-byte	256-byte	28-TSSOP	Small, Low-Cost
ADuC816	Dual 16-bit	Single 12-bit	12-clock 8052	8K-byte	640-byte	256-byte	52-PQFP 56-CSP	Buffered PGA Input
ADuC824	24-bit + 16-bit	Single 12-bit	12-clock 8052	8K-byte	640-byte	256-byte	52-PQFP 56-CSP	Pin-Compatible Upgrade to ADuC816
ADuC831	8-chan 12-bit	Dual 12-bit +Dual PWM	12-clock 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Big-Memory" Upgrade to ADuC812
ADuC832	8-chan 12-bit	Dual 12-bit +Dual PWM	12-clock 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	Same As ADuC831, But With PLL Clock
ADuC834	24-bit + 16-bit	Sngl 12-bit +Dual PWM	12-clock 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Big-Memory" Upgrade to ADuC824
ADuC836	Dual 16-bit	Sngl 12-bit +Dual PWM	12-clock 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Big-Memory" Upgrade to ADuC816
ADuC841 *	8-chan 12-bit	Dual 12-bit +Dual PWM	1-clock 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" Upgrade to ADuC831
ADuC842 *	8-chan 12-bit	Dual 12-bit +Dual PWM	1-clock 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" Upgrade to ADuC832
ADuC843 *	8-chan 12-bit	Dual PWM	1-clock 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	stripped-down ADuC842
ADuC844 *	24-bit + 16-bit	Sngl 12-bit +Dual PWM	1-clock 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" Upgrade to ADuC834
ADuC845 *	10-chan 24-bit	Sngl 12-bit +Dual PWM	1-clock 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" ΣΔ with Multi-Channel Input
ADuC846 *	Dual 16-bit	Sngl 12-bit +Dual PWM	1-clock 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" Upgrade to ADuC836
ADuC847 *	10-chan 24-bit	(none)	1-clock 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	stripped-down ADuC845

Ejemplos



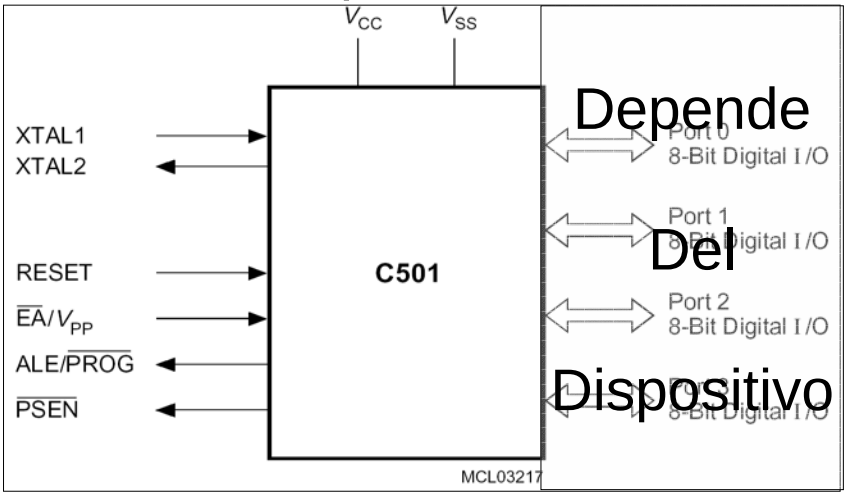
Herramientas

- Compilador / Simulador / Depurador
  - Keil, IAR, Tasking, Raisonance, Crossware, Hi-Tech, SDCC...
- Emuladores
  - Signum, Hitex, Ceibo, Phyton, Metalink, Raisonance, Nohau, Brendes, Isystem…
- Programadores
  - Advantech, Advin, BP, Ceibo, Data I/O, Dataman, Eetools, Elnec, HiLo, ICE technology, Leap, MQP, Needhams, Phyton, Stag, System General, Xeltek...

Características Generales

- Single-Cycle Núcleo 8051: 1MIPS / MHz
- 20 MIPS a 20 MHz @ 2.4V - 5.5V
- 12 Times Faster than Traditional 8051 Core
- Bajo consumo
  - Reducido en 85%
  - Consumo a 3V
    - Modo activo 3 mA @ 12 MHz
    - Modo suspendido 1 mA @ 12 MHz
    - Bajo consumo hasta 1 uA

Arquitectura

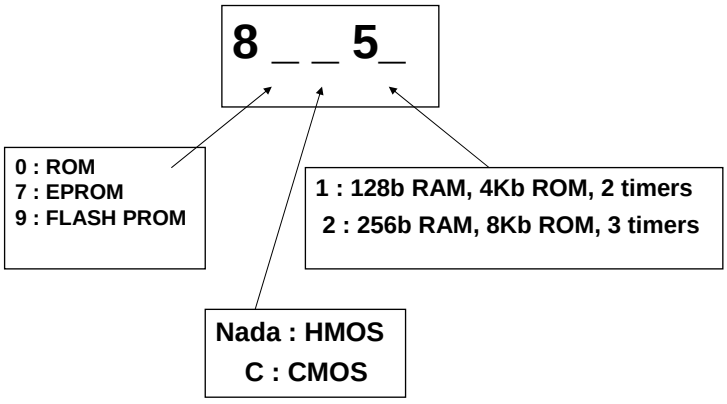


Depende

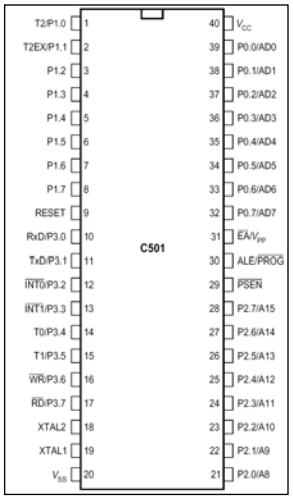
Del

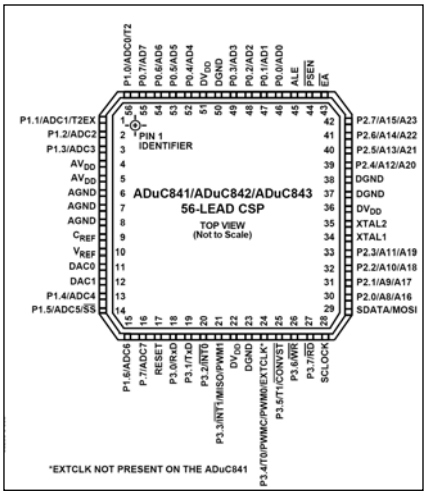
Dispositivo

Identificación y Nomenclatura

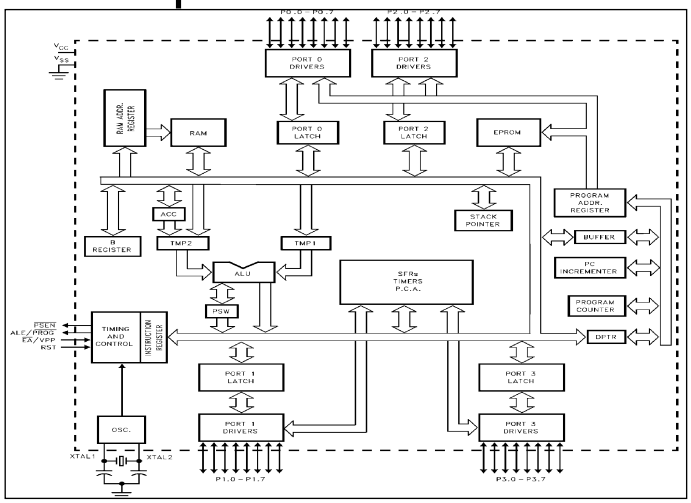


Presentación



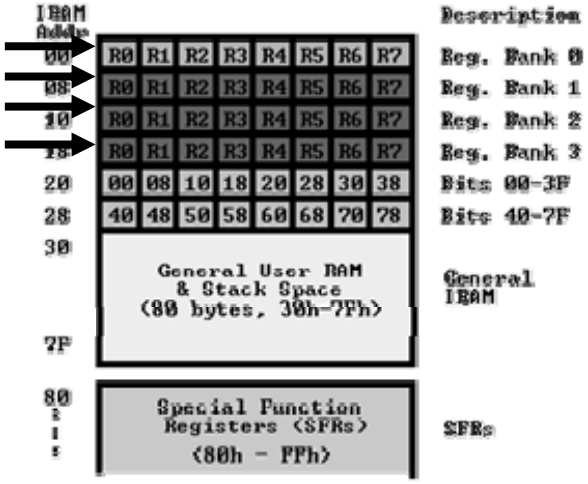


Arquitectura interna

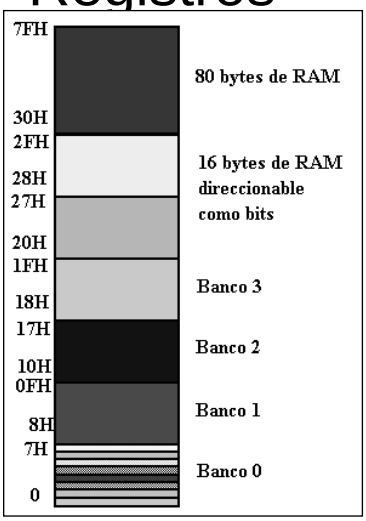


Memoria De datos Interna

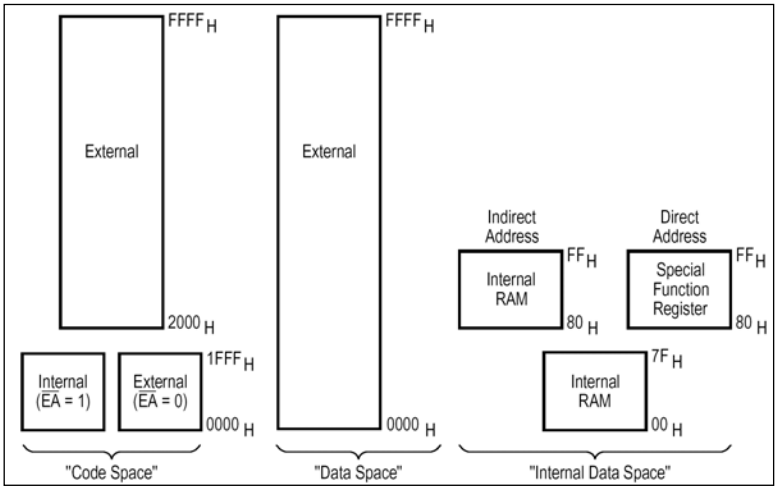
Registros de Propósito general



Registros



Mapas de memoria



Instrucciones

- **ADD A,R4**
- **ADD A,04h**
- **SETB 24h**
- **MOV 20h,#0FFh** Equivale a **SETB 00h**
  SETB 01h
  ……..
  SETB 07h
- **MOV P0,#01h** Equivale a **SETB 80h**

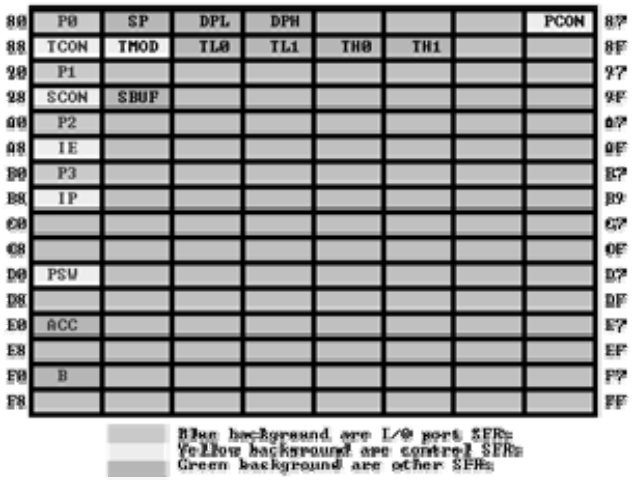
SFRs

Dirección	SFR
80H	P0
81H	SP
82H	DPL
83H	DPH
87H	PCON
88H	TCON
89H	TMOD
8AH	TLO
8BH	TL1
8CH	TH0
8DH	TH1

SFRs

Dirección	SFR
90H	P1
98H	SCON
99H	SBUF
A0H	P2
A8H	IE
B0H	P3
B8H	IP
D0H	PSW
E0H	ACC

SFRs



SFRs

- **P0 (Port 0, Dirección 80h, Bit-Addressable)**
- **SP (Stack Pointer, Dirección 81h) Incrementa**
- **DPL/DPH (Data Pointer Low/High, Direcciones 82h/83h)**
- **PCON (Power Control, Dirección 87h)**
- **TCON (Timer Control, Dirección 88h, Bit-Addressable)**

SFRs

- **TMOD (Timer Mode, Dirección 89h)**
- **TL0/TH0 (Timer 0 Low/High, Dirección 8Ah/8Ch)**
- **TL1/TH1 (Timer 1 Low/High, Dirección 8Bh/8Dh)**
- **P1 (Port 1, Dirección 90h, Bit-Addressable)**

SFRs

- **SCON (Serial Control, Dirección 98h, Bit-Addressable)** Se usan SCON, TCON y TMOD
- **SBUF (Serial Control, Dirección 99h)**
- **P2 (Port 2, Dirección A0h, Bit-Addressable)**
- **IE (Interrupt Enable, Dirección A8h)**
- **P3 (Port 3, Dirección B0h, Bit-Addressable)**
- **IP (Interrupt Priority, Direcciones B8h, Bit-Addressable)**

SFRs

- **PSW (Program Status Word, Direcciónes D0h, Bit-Addressable)**
- **ACC (Accumulator, Dirección E0h, Bit-Addressable)**
- **B (B Register, Dirección F0h, Bit-Addressable)**
- **Los propios de cada Microcontrolador**

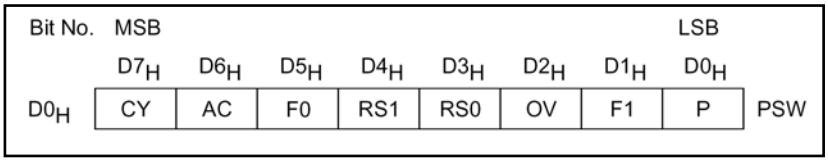
SFRs

- **MOV 50h,#01h**
- **MOV 99h,#01h**

Registros

- Acumulador
- Los Registros R
  - **MOV A,R3**
  - **ADD A,R4**
  - **MOV R5,A**
  - **MOV A,R1**
  - **ADD A,R2**
  - **SUBB A,R5**
- El Registro B
- DPTR
- PC
- SP
- PSW

PSW



PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Manipulación de bits

- **Para conmutar cada bit del Puerto 1 existen 3 modos:**
- **Modo 1: Enviar los datos a P1 a través del ACC**
  - **BACK: MOV A,#55H ;A=01010101B**
    MOV P1,A
    ACALL DELAY
    MOV A,#0AAH ;A=10101010B
    MOV P1,A
    ACALL DELAY
    SJMP BACK

Manipulación de bits

- **Modo 2: Acceder al Puerto 1 directamente**

```
BACK:   MOV     P1,#55H  ;P1=01010101B
        ACALL   DELAY
        MOV     P1,#0AAH ;P1=10101010B
        ACALL   DELAY
        SJMP    BACK
```

- **Modo 3: Read-modify-write**

```
        MOV     P1,#55H  ;P1=01010101B
AGAIN:  XRL   P1,#0FFH
        ACALL   DELAY
        SJMP    AGAIN
```


Manipulación de bits

(a) Observar el estado de P1.2 hasta que pase a alto.
(b) Cuando P1.2 pase a alto, escriba 45H al puerto 0 y
(c) Genere un pulso alto a bajo en P2.3.

```
        SETB  P1.2          ;programo P1.2 como entrada
        MOV   A,#45H        ;A=45H
AGAIN:
        JNB   P1.2,AGAIN    ;salir cuando P.2=1
        MOV   P0,A          ; sacar A a P0
        SETB  P2.3          ; P2.3 alto
        CLR   P2.3          ; Transición H-L en P2.3
```

Modos de Direccionamiento

- **Direccionamiento Inmediato:** MOV A,#20h
- **Direccionamiento Directo:** MOV A,30h (SFRs)
- **Direccionamiento Indirecto:** MOV A,@R0
- **Externo Directo:** MOVX A,@DPTR
- **Código Indirecto:** MOVC A,@A+DPTR

Saltos

- Condicionales

```
        JB      45h,PEPE
        NOP
PEPE:....
```

- Directos

```
        LJMP  Por_ahi
        ……..
Por_ahi:
```

- **SJMP** (+127/-128)
- **AJMP** (2K)

Subrutinas

- LCALL
- RET

Diagrama Circuital-Mem. Prog. Externa

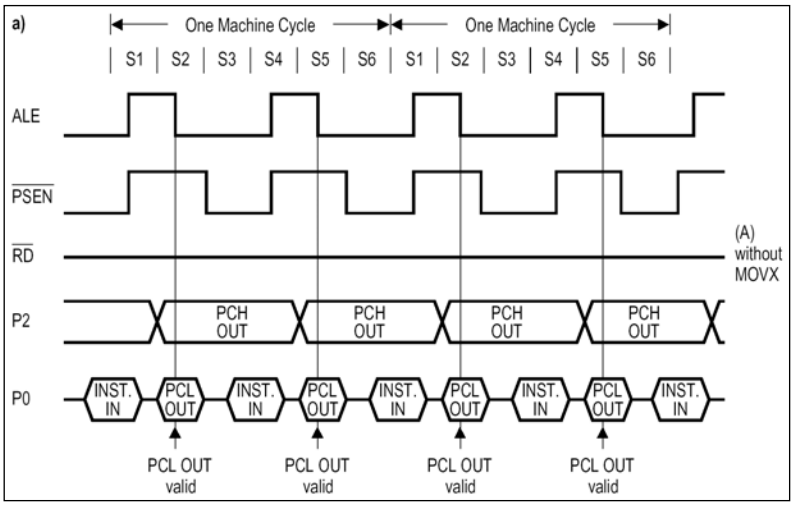


Diagrama Circuital-Mem. Prog. Externa

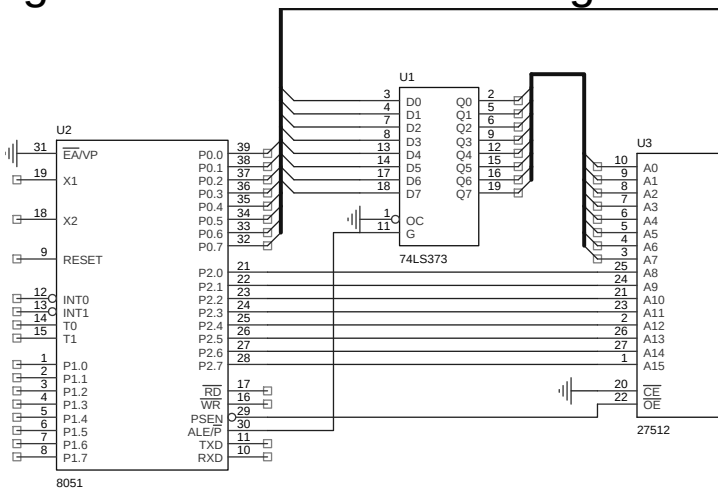


Diagrama Circuital-Mem. Datos Externa

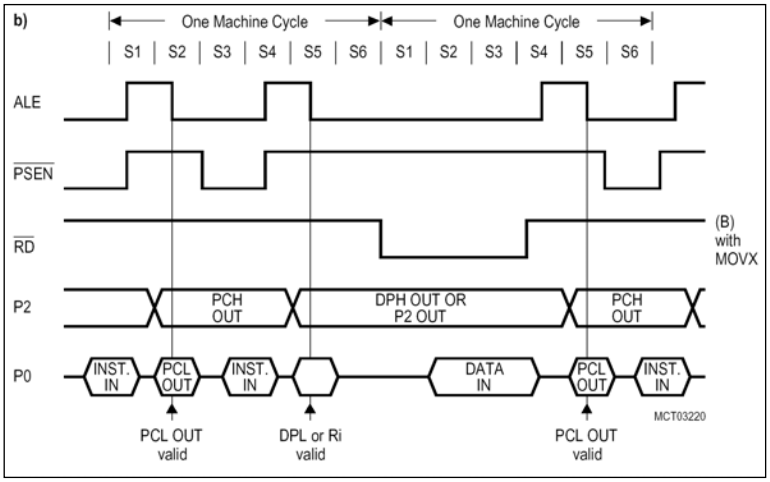


Diagrama Circuital-Mem. Datos Externa

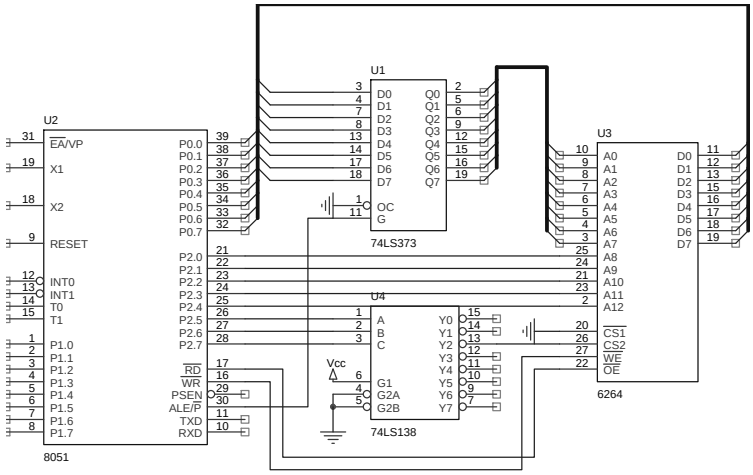
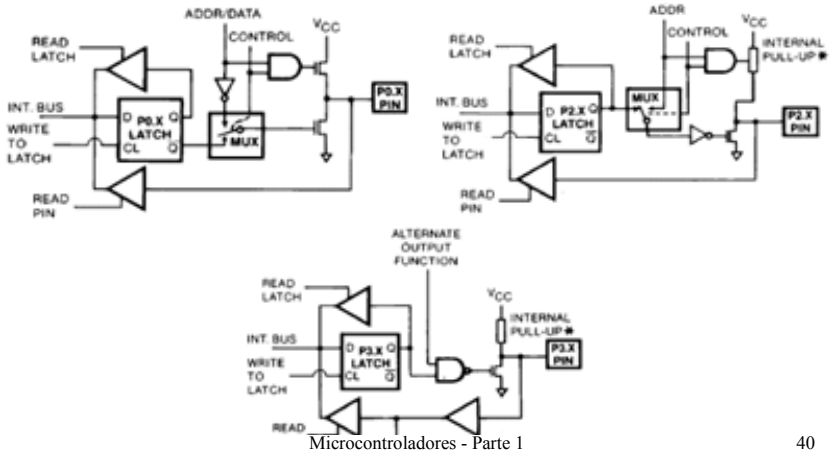
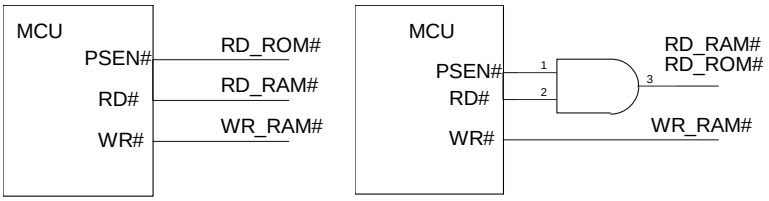


Diagrama de las patas



Selección de memorias



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